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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/539,314
Filing Date: June 15, 2005
Appellant(s): WEEKAMP ET AL.

Dicran Halajian
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/30/2007 appealing from the Office action mailed 05/31/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-10.

Claims 11-12 have been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,324,072	Lorentz et al.	03-1999
2002/0117743	Nakatani et al.	12-2001
4,897,327	Dubin et al.	05-1988

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3,5,6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743)

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Re. Claim 1, Lorentz et al. discloses an electronic device comprising the steps of:

providing a substrate having a substrate (same as first layer of an electro conductive material)(3), in which layer patterns are defined in accordance with desired pattern;

providing a foil having a second substrate (same as second patterned layer of electro conductive material), in which layer conductors are defined in accordance with a desired pattern;

Providing elements, include semiconductor chips (same as semiconductor elements) and a first conductor track plane (same as first connection element)(3) on the first side of the substrate, thereby bringing the first conductor track plane (same as first connection element)(3) and conductors in the first layer into electric contact; and also establish a electric contact between the second conductor track planes (same as second connection element)(6) and the corresponding conductors in the second layer(5).

Lorentz et al. does not teach having the encapsulation and separating the assembly of substrate.

However, Nakatani et al teaches separating the assembly of substrate and encapsulation as can be seen in figure 7H.

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to separate the assembly of substrate to repair bad components on the release layer (same

as assembly of substrate) and to encapsulate the elements to manufacture the semiconductor device.

Re. Claim 2, Lorentz et al. disclose all the limitations except removing the detachable layer.
However, Nakatani et al. discloses removing the release carrier (710)(same as detachable layer).
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to remove the detachable layer to coat the organic film.

Re. Claim 3, Lorentz et al. discloses a foil comprising a second substrate (same as patterned layer)(5) and the foil are provided in such a manner that the second patterned layer faces the elements (Figure 1). It is apparent to have the foil comprising a electrically isolating layer otherwise the device will be short circuited.

Re. Claim 5, Lorentz et al. disclose all the limitations except having the connection conductors already defined in the first layer.

However, Nakatani et al. teaches having the wiring patterns (same as connection conductor) defined in the first layer (701)(figure 7A).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to have the connection conductors already defined in the first layer to have better thermal stress.

Re. Claim 6, Lorentz et al. disclose all the limitations except removing the sacrificial layer.
However, Nakatani et al. discloses removing the release carrier(710)(same as sacrificial layer) after the provision of passivating material. It is apparent to undergo the provision of passivating material to encapsulate the elements.
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to remove the sacrificial layer to manufacture the semiconductor device.

Re. Claim 7, Lorentz et al. does not teach having the encapsulation.

However, Nakatani et al teaches encapsulation of the sheet material (same as second patterned layer) and that the substrate has contact faces (709) for external contacting are situated on the second side facing the first side and can be seen in figure 7I.

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to separate

the assembly of substrate to repair bad components on the release layer (same as assembly of substrate) and to encapsulate the elements to manufacture the semiconductor device.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743) as applied to claim 1 and further in view of Dubin et al(US 4,897,327).
Re. Claim 4, Lorentz et al. discloses the foil provided in such a manner that the second patterned layer faces the elements (Figure 1).
Lorentz et al. does not teach having a electrically isolating gauze.
However, Dubin et teaches having a fiber glass board(same as electrically isolating gauze).
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. and Dubin et al. to have a electrically isolating gauze to make integrated circuit boards.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743).

Re. Claim 8, Lorentz et al. discloses a electronic device comprising the steps of:

providing a substrate having a substrate (same as first layer of an electro conductive material)(3), in which layer patterns are defined in accordance with desired pattern;

providing a foil having a second substrate (same as second patterned layer of electro conductive material), in which layer conductors are defined in accordance with a desired pattern;

Providing elements, include semiconductor chips(same as semiconductor elements) and a first conductor track plane(same as first connection element)(3) on the first side of the substrate, thereby bringing the first conductor track plane(same as first connection element)(3) and conductors in the first layer into electric contact; and also establish a electric contact between the second conductor track planes(same as second connection element)(6) and the corresponding conductors in the second layer(5).

Lorentz et al. does not teach having the encapsulation.

However, Nakatani et al teaches encapsulation which is provided from second side of the electronic device through the second patterned layer(Fig 7H).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to encapsulate the elements to manufacture the semiconductor device.

Re. Claim 9, Lorentz et al. discloses the second substrate (same as second conductive layer) on the side facing away from the elements. It is apparent to have the foil comprising a patterned isolating layer otherwise the device will be short-circuited.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743) as applied to claim 8 and further in view of Dubin et al(US 4,897,327).
Re. Claim 10, Lorentz et al. discloses all the limitations as discussed in claim 8, but does not teach having gauze of isolating material.
However, Dubin et teaches having a fiber glass board(same as isolating gauze). It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. and Dubin et al. to have a gauze of isolating material to make integrated circuit boards.

(10) Response to Argument

In response to appellant arguments, Page 10,lines 12-15, ...Nakatani does not teach providing a passivating material from the second side of the semiconductor element through the foil, which passivating material forms an encapsulation of the elements..., it is clear from Figure 7H of Nakatani that the passivating film (704) from the second side of the semiconductor element(702 or 703) through the foil (701,711 and 708), which passivating material forms an encapsulation of

the elements(703 or 702), which makes it clear that the limitation in the claim read on the Nakatani et al. reference.

In response to appellant's arguments, Page 11,lines 1-3, "... Nakatani vias 705,708 filled with the conductive paste does not provide isolation...", the claim does not mention this limitation.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ankush k Singal/

Examiner, Art Unit 2895

Conferees:

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895

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/R. L. M./
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